REMARKS

Claims 1 and 7 have been amended and claims 6 and 9 have been canceled in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **July 16, 2003**.

Claim Rejections under 35 USC §102

Claims 1-5 and 7 are rejected under 35 USC §102(e) as being anticipated by US Patent No. 6,544,845 to Yoo et al.

Claim 1 is clarified in that an impurity concentration of a source region of said nonvolatile memory device is increased so as to reduce concentration of an electric field on an edge of the floating gate electrode, the concentration of the electric field being caused by a high voltage applied to the source region at a time of erasing an electric charge from said nonvolatile memory device and the bird's beak structure increases a thickness of the tunnel insulating film at the edge of the floating gate electrode so as to prevent the tunnel insulating film from being degraded by the concentration of the electric field on the edge of the floating gate electrode.

Although a bird's beak structure and such an impurity concentration of a source region may seem conventional, the present invention is unconventional because it realizes an improvement in the reliability of a device by effectively using the bird's beak structure and the

impurity concentration of a source region in combination. Specifically Claim 1 has further incorporated the features of

> "an impurity concentration of a source region of said nonvolatile memory device is increased so as to reduce concentration of an electric field on an edge of the floating gate electrode, the concentration of the electric filed being caused by a high voltage applied to the source region at a time of erasing an electric charge from said nonvolatile memory device; and
>
> the bird's beak structure increases a thickness of the tunnel insulating film at the edge of the floating gate electrode so as to prevent the tunnel insulating film from being degraded by the concentration of the electric field on the edge of the floating gate electrode."

By so amending, it is believed that claims 1-5 and 7 are allowable over Yoo.

Claim Rejections under 35 USC §103

Claim 6 is rejected under 35 USC §103(a) as being unpatentable over US Patent No. 6,544,845 to Yoo in view of US Patent No. 6,436,765 to Lion et al.

Claim 8 is rejected under 35 USC §103(a) as being unpatentable over US Patent No. 6,544,845 to Yoo in view of Applicant Admitted Prior Art.

Since claims 6 and 8 depend on independent claim 1, it is believed that claims 6 and 8 should be allowed once the rejection of claim 1 is withdrawn.

New Claim

New independent claim 40 is added as shown so as to further clarify the subject matter of the present invention over Yoo.

In the present invention, it is apparent that the gate electrode and the control gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant are neither disclosed nor taught in Yoo.

Claim 40 includes the limitations of claims 1-3, which are neither disclosed nor suggested in Yoo. Accordingly, it is believed that claim 40 is allowable over Yoo.

Claim Rejections under 35 USC §112

Claims 9-15 are rejected under 35 USC §112, first paragraph.

As to this rejection, we have reviewed the response dated May 6, 2003 to the first Office Action dated February 6, 2003, and have found in page 6 of Remarks that a first active region and a second active region are indicated erroneously as 11a and 11b. They should be 11A and 11B. Accordingly, that portion of the Remarks has been amended as shown herein below.

Independent claim 9 is supported by way of an example in Figure 12 and associated written specification. There is indeed disclosed a semiconductor integrated circuit device comprising a substrate (11); a nonvolatile memory device (flash memory) formed in a memory cell region (Region A) of said substrate, the nonvolatile memory device comprising a first active region (11A) covered with a tunnel insulating film (12A); a second active region (11B) formed next to the first active region (11A) and covered with an insulating film (12A, 12C); a control gate formed of an embedded diffusion region (11c) formed in the second active region; a first gate electrode (13A) extending on the tunnel insulating film (12A) in the first active region (11A) and forming a bridge between the first and second active regions to be capacitive-coupled

via the insulating film (12A, 12C) to the embedded diffusion region (11c) in the second active region (11B), the first gate electrode (13A) having sidewall faces thereof covered with a protection insulating film (18) formed of a thermal oxide film; and a diffusion region (11a, 11b, 11c) formed on each of sides of the first gate electrode (13A) in the first active region (11A); and a semiconductor device (MOS transistor) formed in a device region (Regions B, C) of said substrate, the semiconductor device comprising a gate insulating film (12B) covering said substrate and a second gate electrode (13B) formed on the gate insulating film (12B), wherein a bird's beak structure is formed of the thermal oxide film (18) at an interface of the tunnel insulating film (12A) and the first gate electrode (13A), the bird's beak structure penetrating into the first gate electrode (13A) along the interface from the sidewall faces of the first gate electrode; and the gate insulating film (12B) is interposed between said substrate (11) and the second gate electrode (13B) to have a substantially uniform thickness.

By so amending, claims 9-15 are placed in condition for allowance. Reconsideration and withdrawal of this rejection are respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, all pending claims are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

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